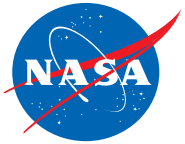

First-Order SPICE Modeling of Extreme-Temperature 4H-SiC JFET Integrated Circuits

Philip G. Neudeck, David J. Spry
NASA Glenn Research Center, Cleveland, Ohio USA

Liangyu Chen
Ohio Aerospace Institute, Cleveland, Ohio USA

2016 IMAPS Interrnational High Temerature Electronics Conference
Albuquerque, New Mexico USA
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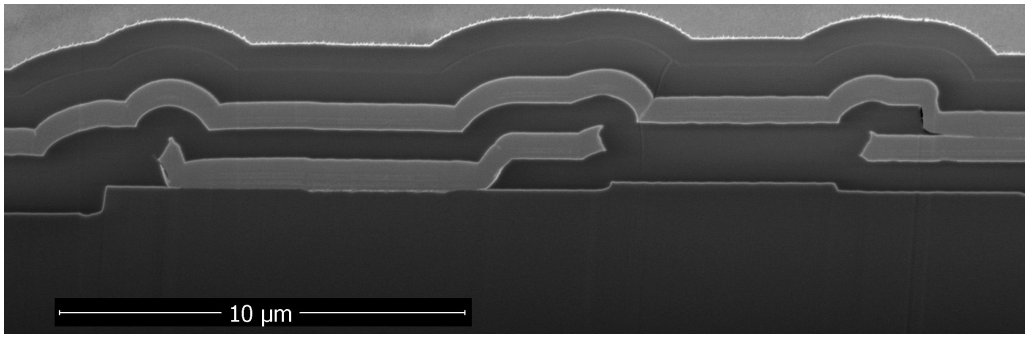
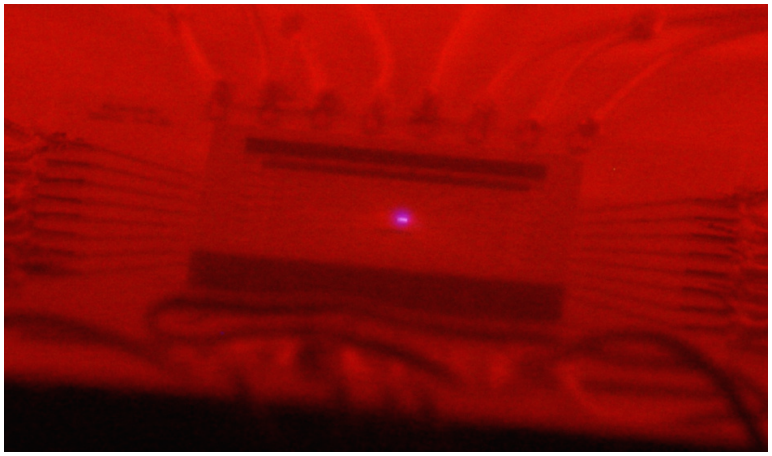
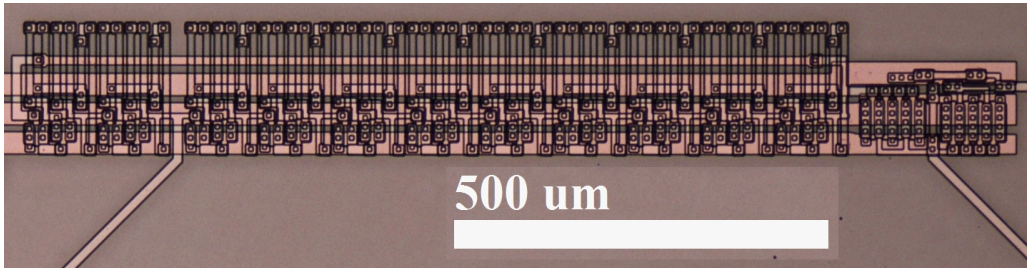
Progress in 500 °C Durable 4H-SiC JFET ICs

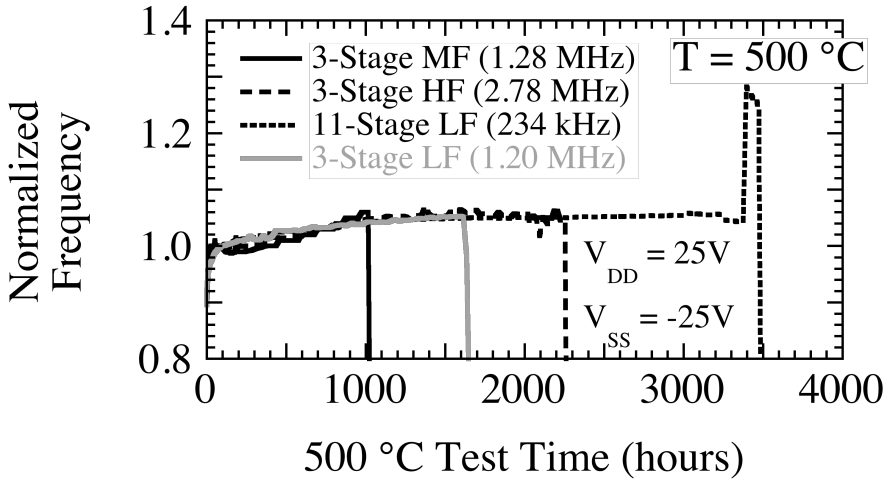
(D. Spry et. al., HiTEC 2016 & SPIE 2016 presentations)

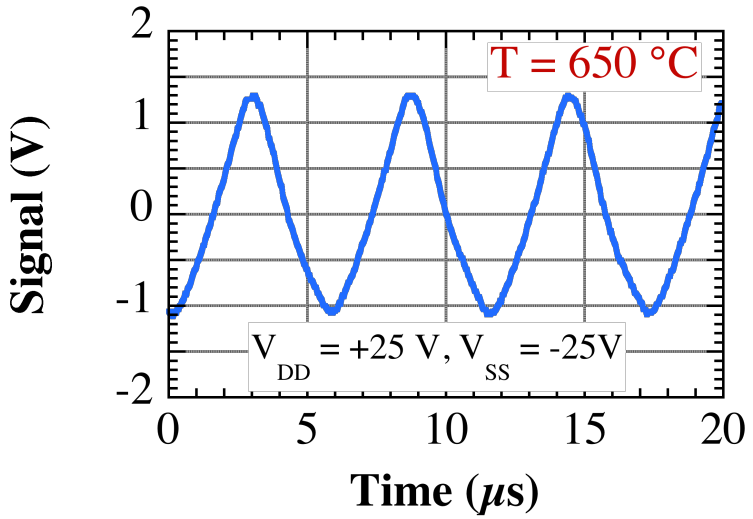
Durable 2-Level Interconnect IC Process for More Capable T ≥ 500 °C ICs











Outline

Goal: Enable anyone to SPICE-model 500 °C durable integrated circuit designs for their application.

500 °C Durable Integrated Circuit Technology Background
- Device Approach (n-JFETs and n-resistors in 4H-SiC)
- Circuit Approach (Ratio-based circuit designs)
- SPICE Approach (Model JFETs using NMOS Level 1)

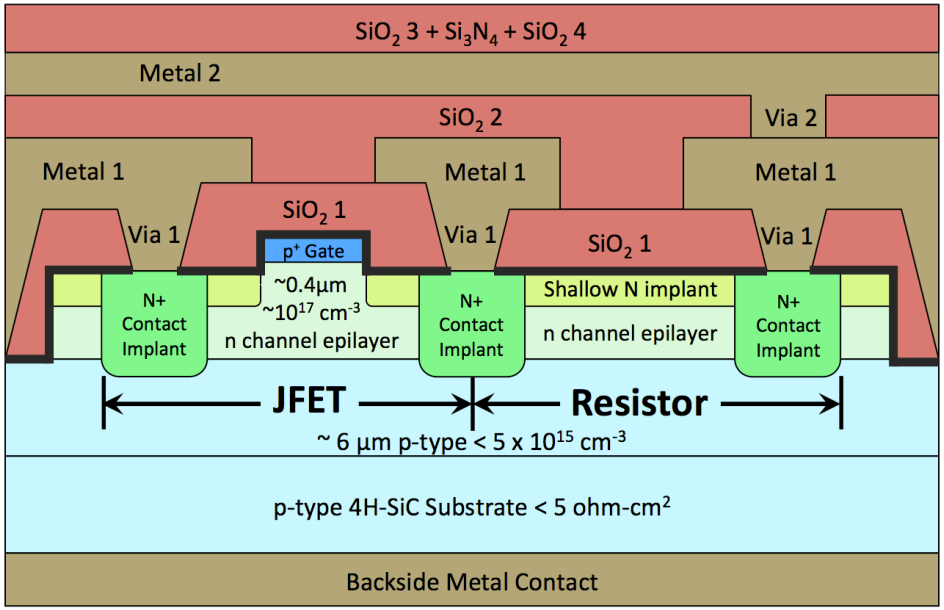
Experimental Device Parameter Measurements
- Dependence on Position on the SiC Wafer
- Dependence on Temperature

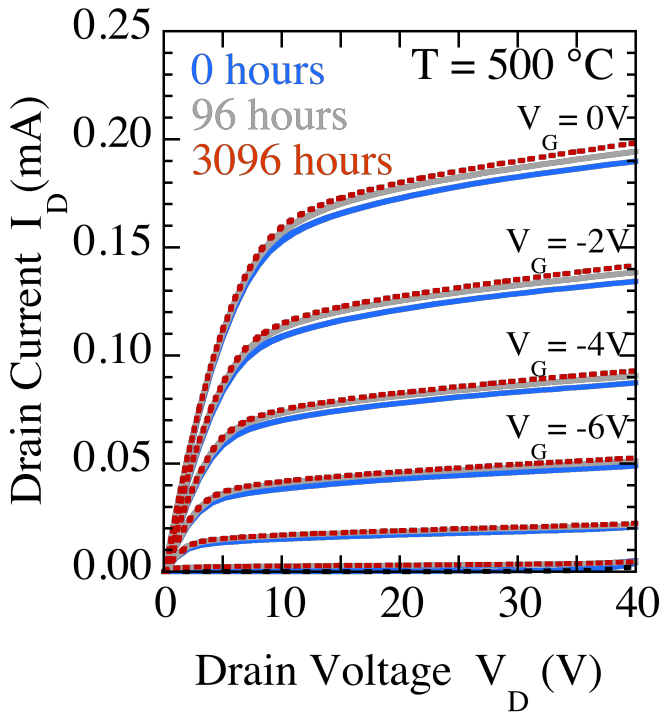
SPICE Models
- JFETs & Resistors, vs. Wafer Position and vs. Temperature.
- Comparison of SPICE-Modeled vs. Measured

Device Approach

Most applications require long-term circuit operation.

SiC n-JFETs and n-resistors offer the highest durability and stability for long-term circuit operation at T ≥ 500 °C.

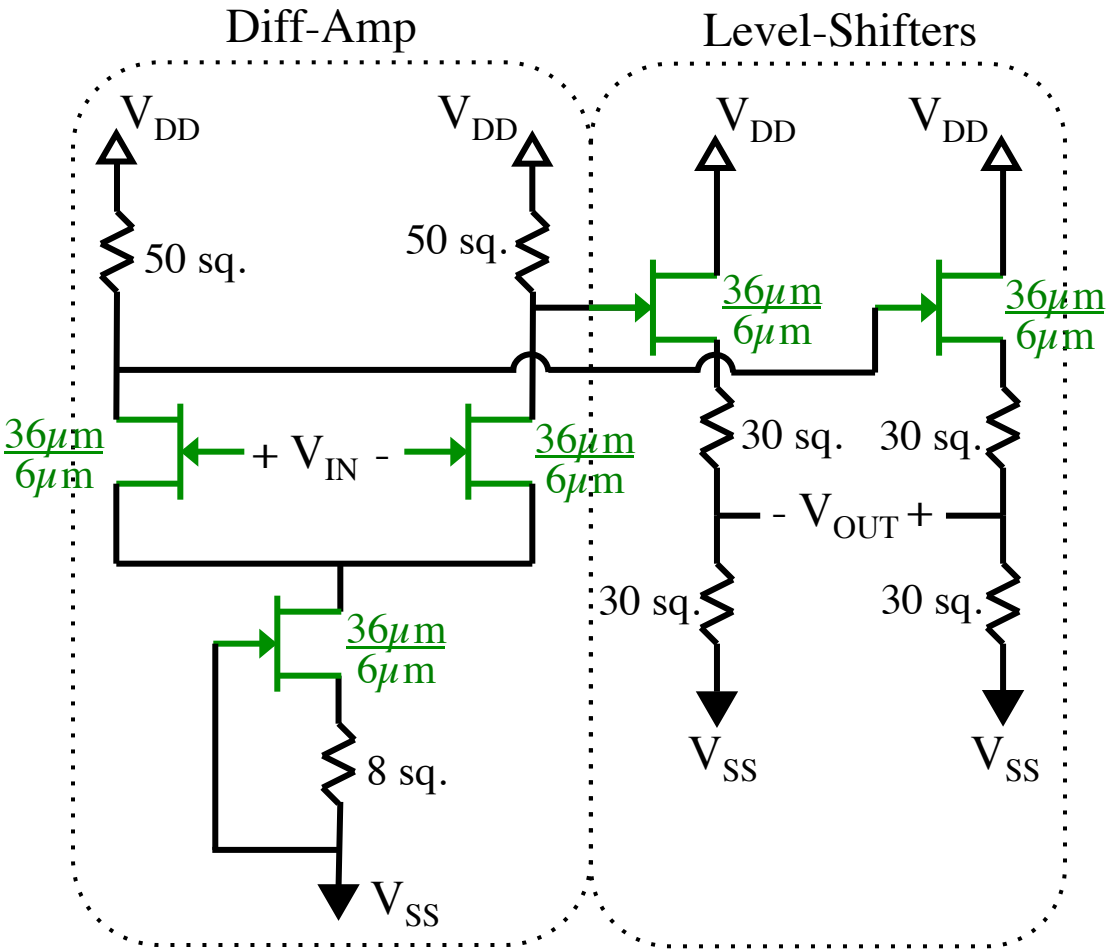


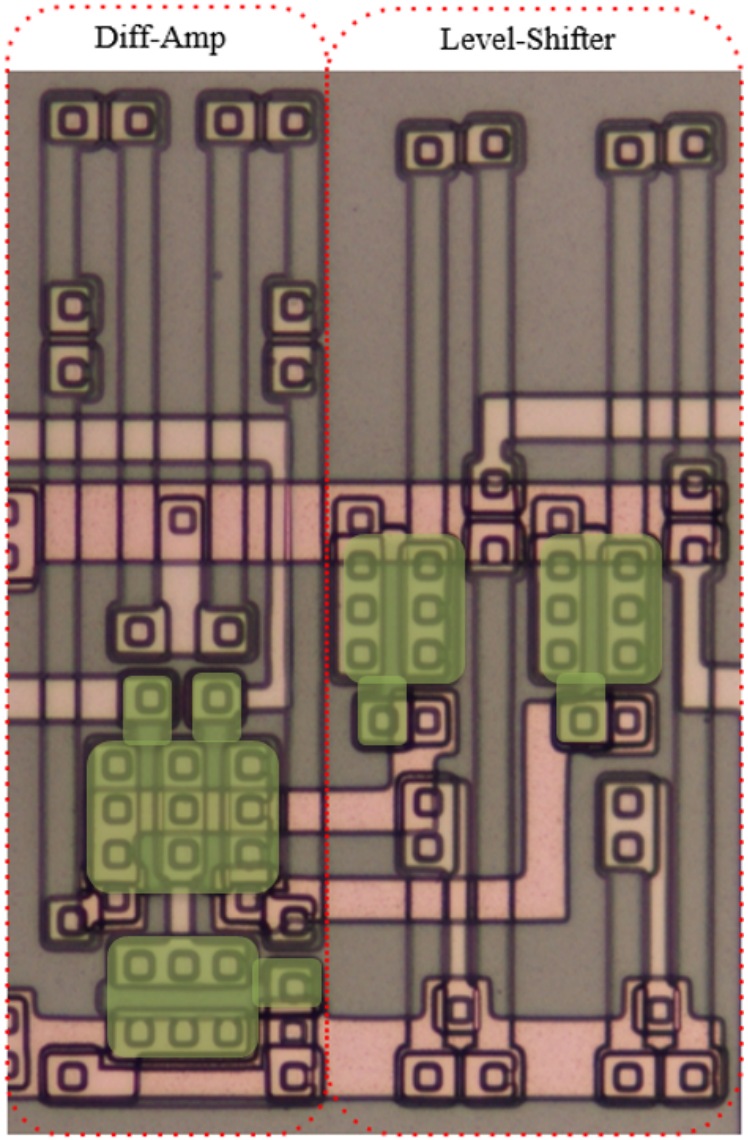


Other device structures and materials have yet to demonstrate 1000+ hours of 500 °C stable electrical operation.

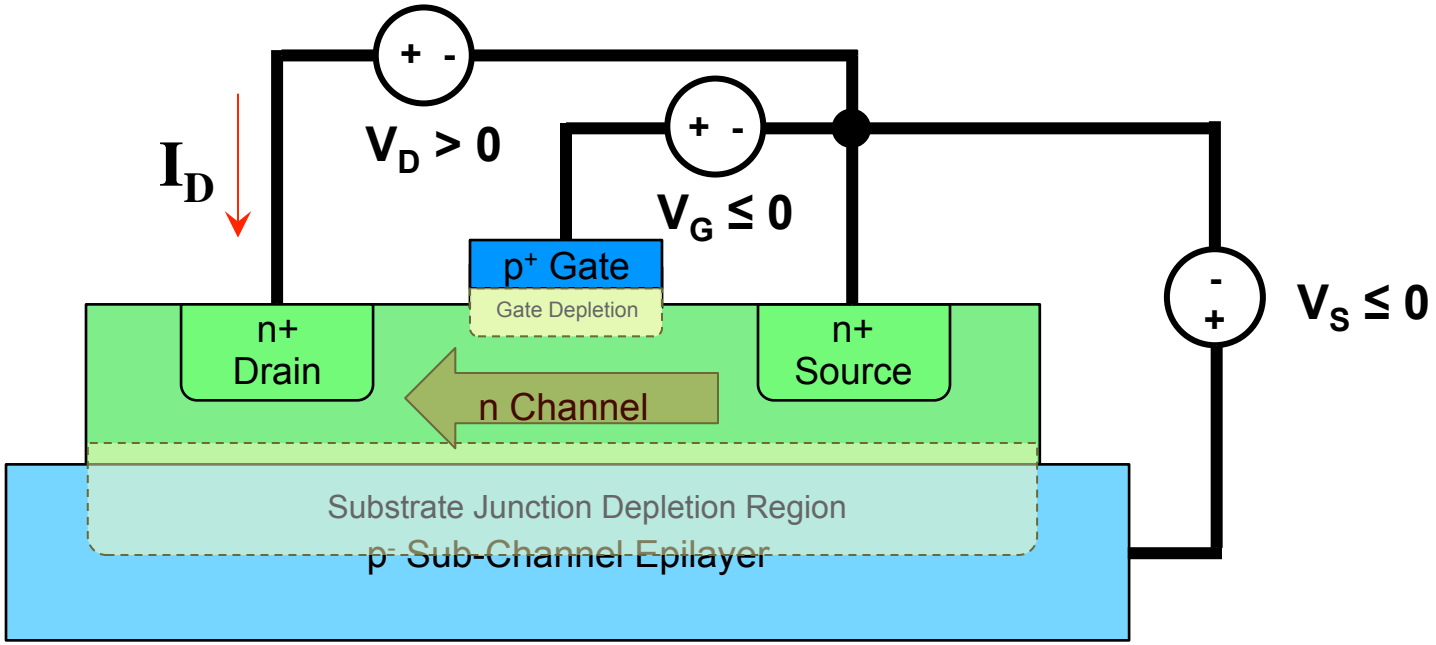
Circuit Approach

All integrated circuits of this work are comprised of interconnected 4H-SiC n-JFET's and 4H-SiC n-resistors.





N-Channel JFET Bias Limitations



N-channel electron current flow from Source to Drain is modulated by Gate voltage V_G.

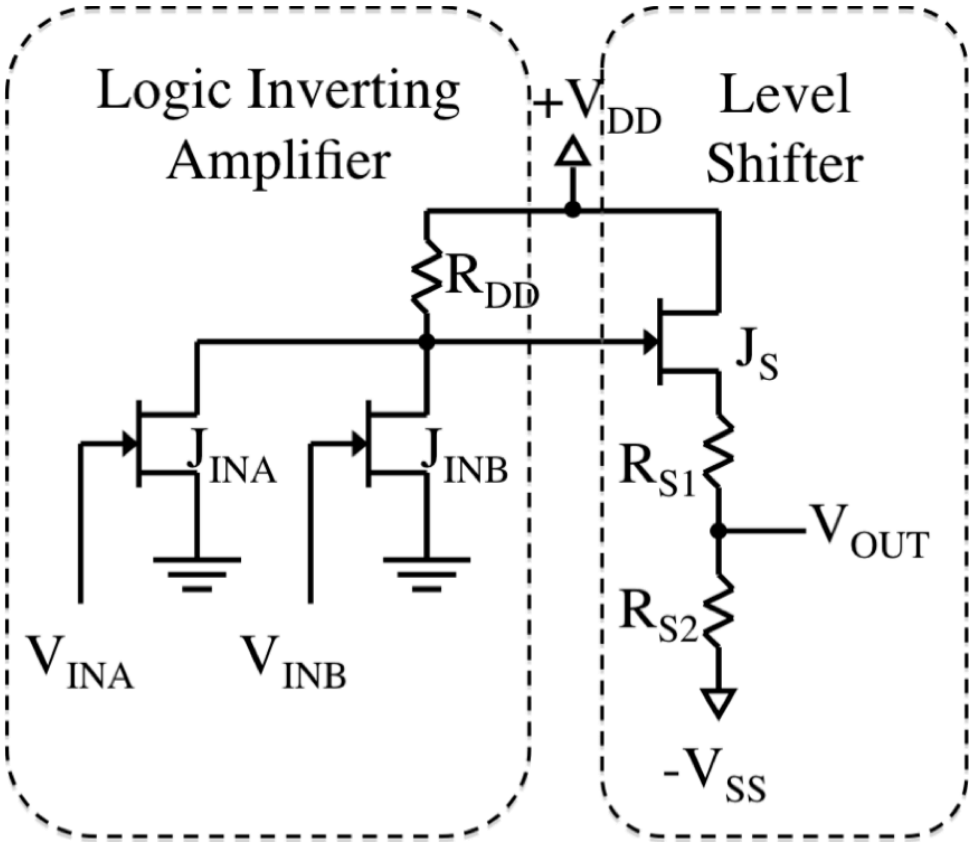
JFETs are "normally ON" - n-channel is "on" to current flow at $V_G = 0$ V.
- Turn-off requires application of $V_G \leq V_T$ "Threshold Voltage" < 0 V.
- N-channel epilayer control is not yet sufficient for "normally OFF" JFET approach.

Forward bias of gate pn junction and substrate pn junction is to be avoided.
- Keeps desired signal currents confined/isolated to n-channel.

SiC JFET Logic Gate Circuit

"Layout ratio" approach to circuit design enables circuits to function over a wide range of temperature and wafer process variations.

M. Krasowski, US Patent 7,688,117



Power: $+V_{DD}$, GND, $-V_{SS}$
p-type Substrate bias = $-V_{SS}$

Nominal Implementation
$|V_{DD}| = |V_{SS}| > 2 \times |V_T|$
$R_{DD} = R_{S1} = R_{S2} >> V_{DD}/I_{DSS}$
V_{HIGH} ~ GND
V_{LOW} ~ 0.5 x V_{SS} (negative)

Negative logic levels and substrate bias ensure JFET p^+ gate to n-channel "gate diodes" AND n-channel to p-substrate "substrate diodes" are REVERSE BIASED.

With large substrate bias, "body bias effect" impacts device & circuit characteristics.

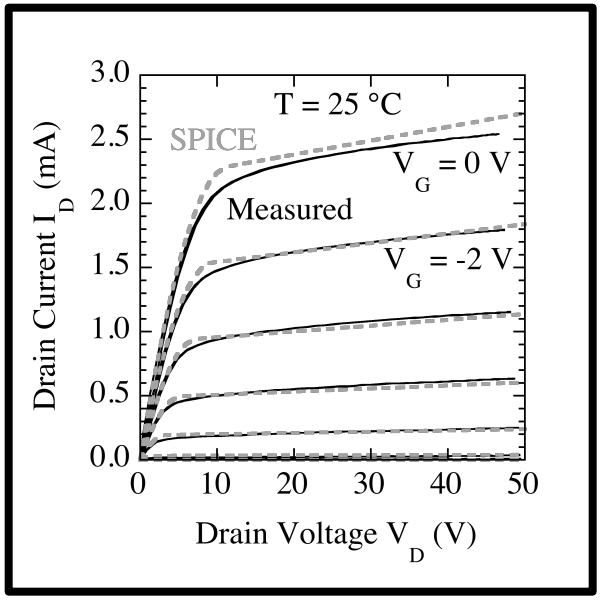
SPICE Modeling Approach

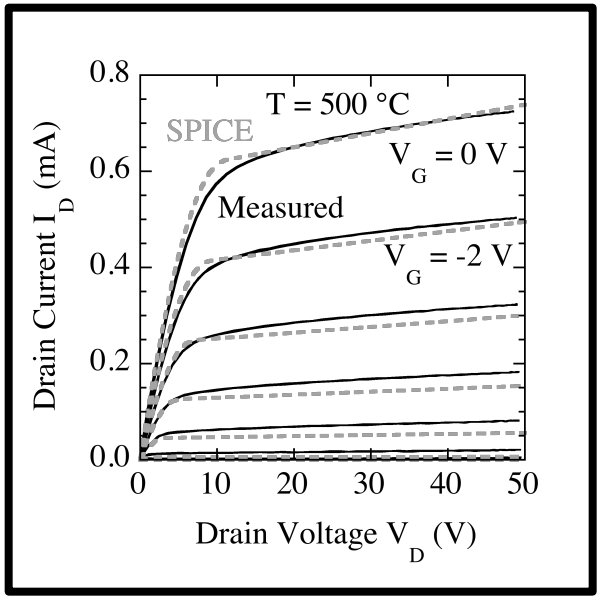
Many different SPICE versions and enhancements are available, but most share “baseline” features and device models from original SPICE version (developed at UC Berkeley).

However, baseline version SPICE JFET model **DOES NOT include body bias effect.**

Baseline SPICE NMOS LEVEL 1 model (n-channel MOSFET, that includes body effect) can be employed to model SiC JFET’s to first-order accuracy PROVIDED:

- Forward bias IS AVOIDED for gate and substrate pn junctions.
- Adjusted NMOS model parameters are used for high-temperature simulation.
  - Baseline SPICE NMOS crashes when TEMP parameter approaches 300 °C.





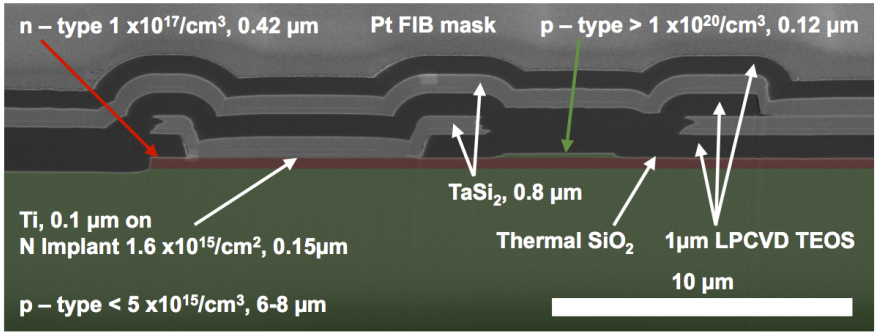
Neudeck et. al.,
HiTEC 2008
6H-SiC JFET modeling via source-code modified NGSPICE NMOS Level 1

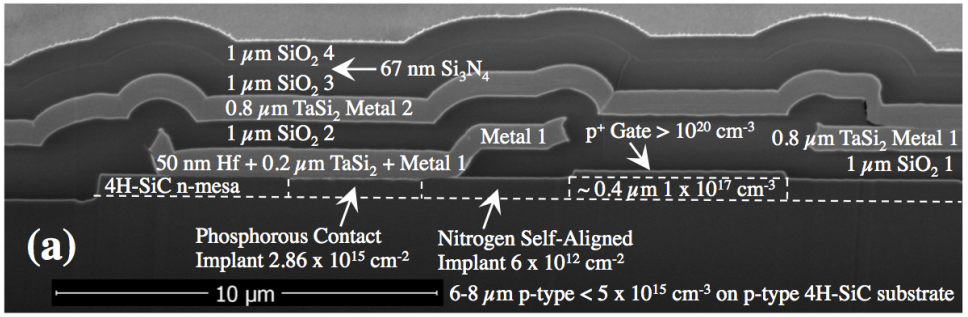
Experimental

SPICE models have been developed based on measured results from the two most recent NASA Glenn 4H-SiC JFET IC wafer process runs.

6 µm feature size process, implemented on 76 mm diameter commercial 4H-SiC epiwafers.

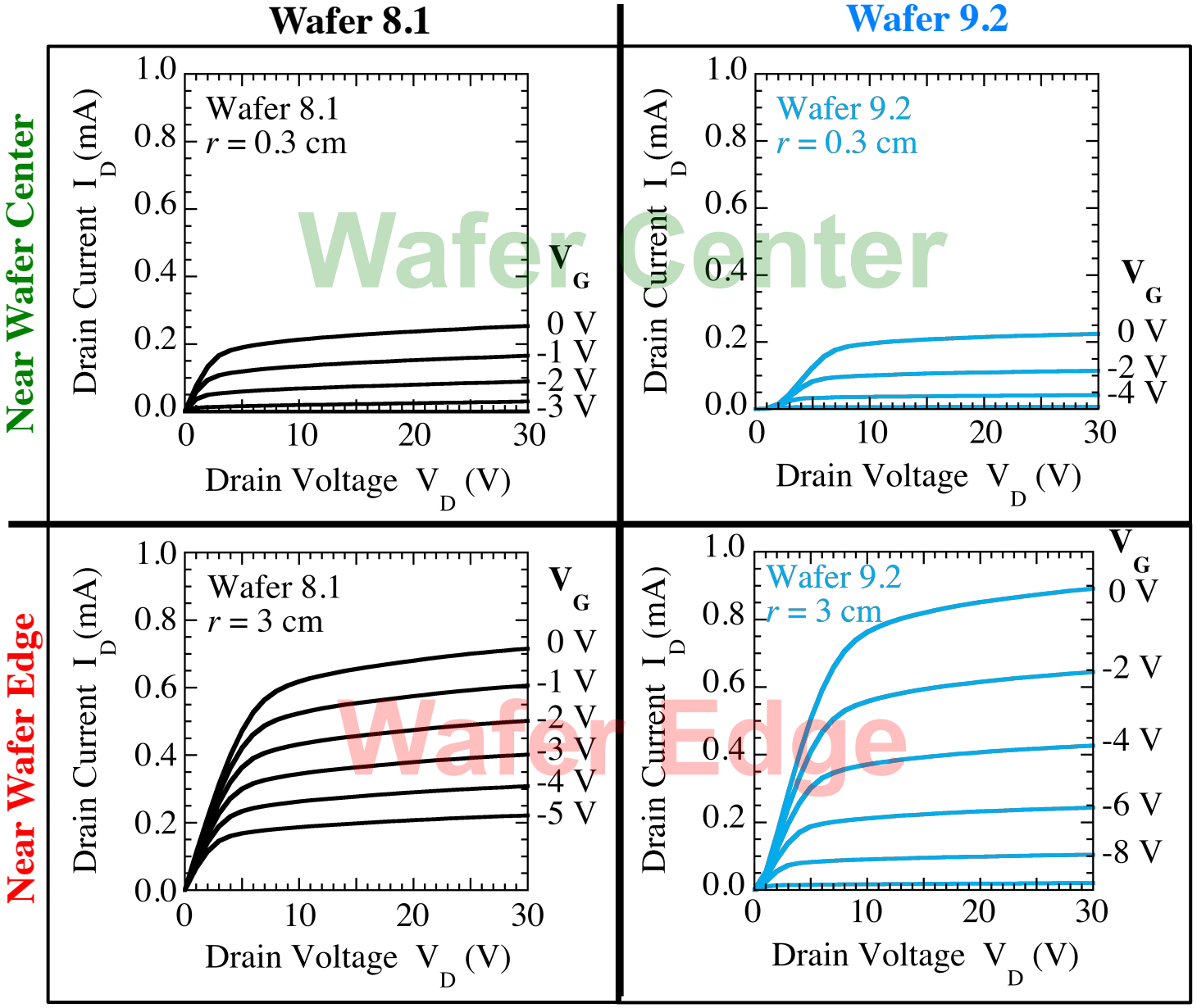
NASA "Wafer 8.1" [1,2]	Major Process Difference	NASA "Wafer 9.2" [3]
2008	Epiwafer Purchase	2014
Titanium	SiC Ohmic Contact Metal	Hafnium
Nitrogen Dose 1.6 x 10^{15} cm^{-2}	Source/Drain Implant	Phosphorus Dose 2.9 x 10^{15} cm^{-2}
1µm SiO_2	Top Dielectric Passivation Stack	1µm SiO_2 + 67nm Si_3N_4 + 1µm SiO_2





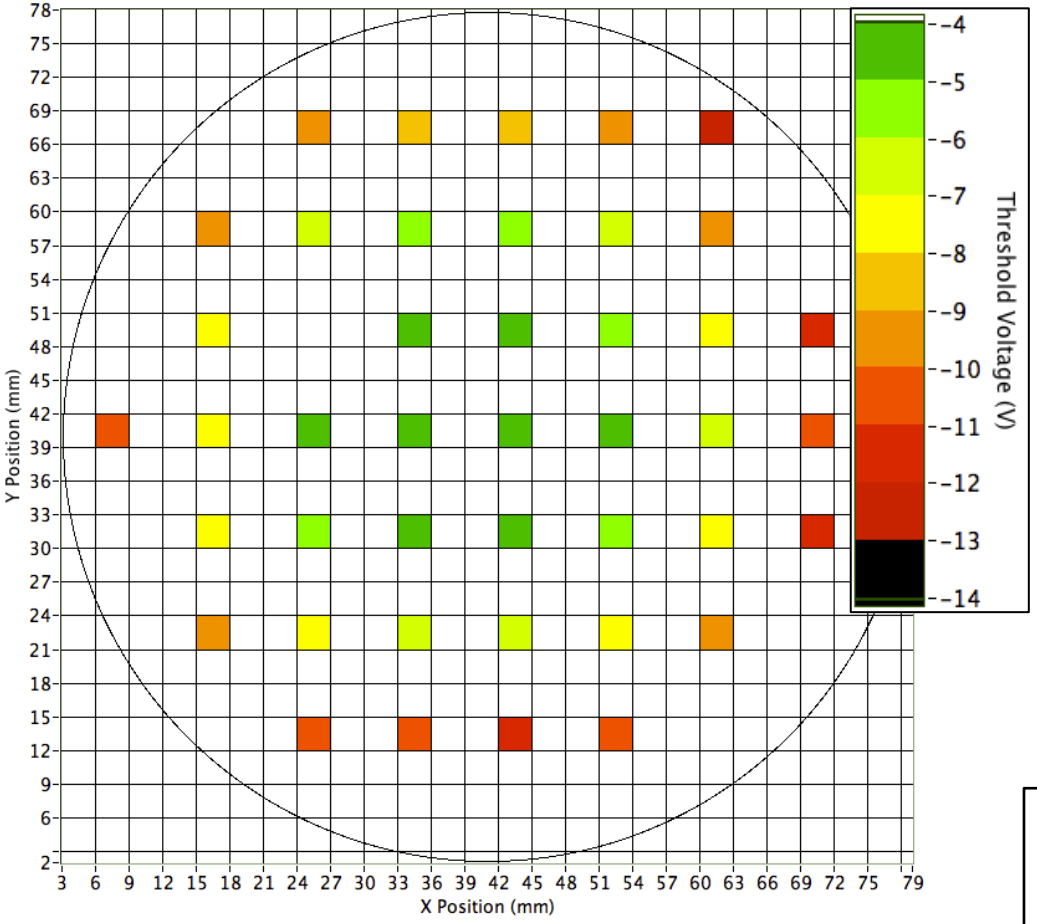
[1] D. Spry et. al., Materials Science Forum **858** p. 908 (2016).
[2] D. Spry et. al., Materials Science Forum **858** p. 1112 (2016).
[3] D. Spry et. al. IEEE Electron Device Letters **37(5)** p. 625 (2016).

Measured 25 °C JFET Characteristics

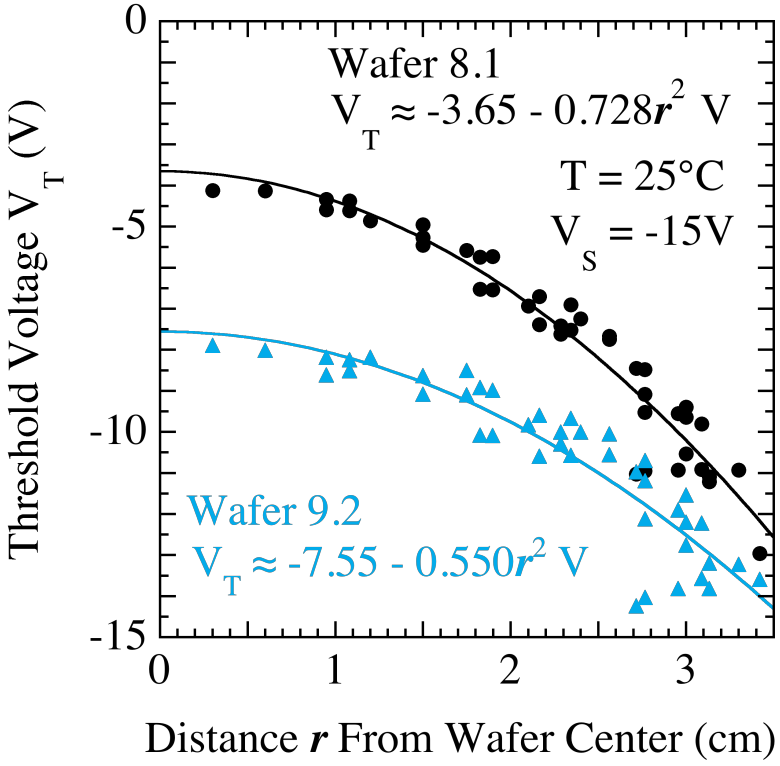


Experimental JFET Threshold (V_T) Non-Uniformity

Wafer Probe Map of Wafer 8.1 JFET V_T
T = 25 °C, V_D = 20V, V_S = -15V
(76 mm diameter wafer)



Plot of Measured JFET V_T
vs. Radial Distance (***r***)
from Wafer Center

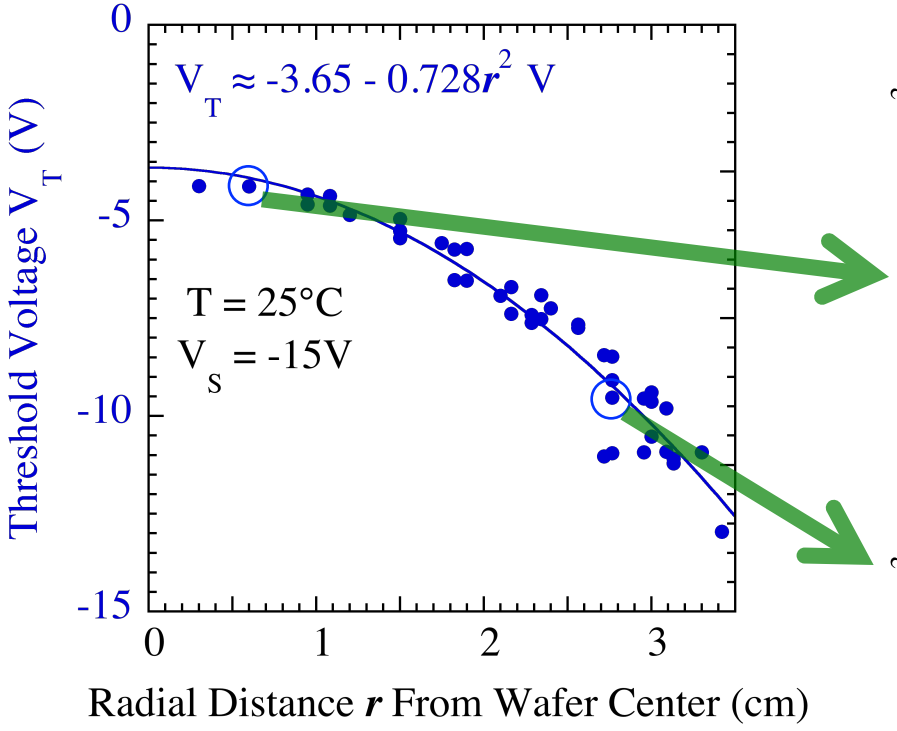


Positional variation of JFET V_T is radial and due to non-uniformity in as–grown epilayers.

[1] Materials Science Forum **858** p. 903 (2016).

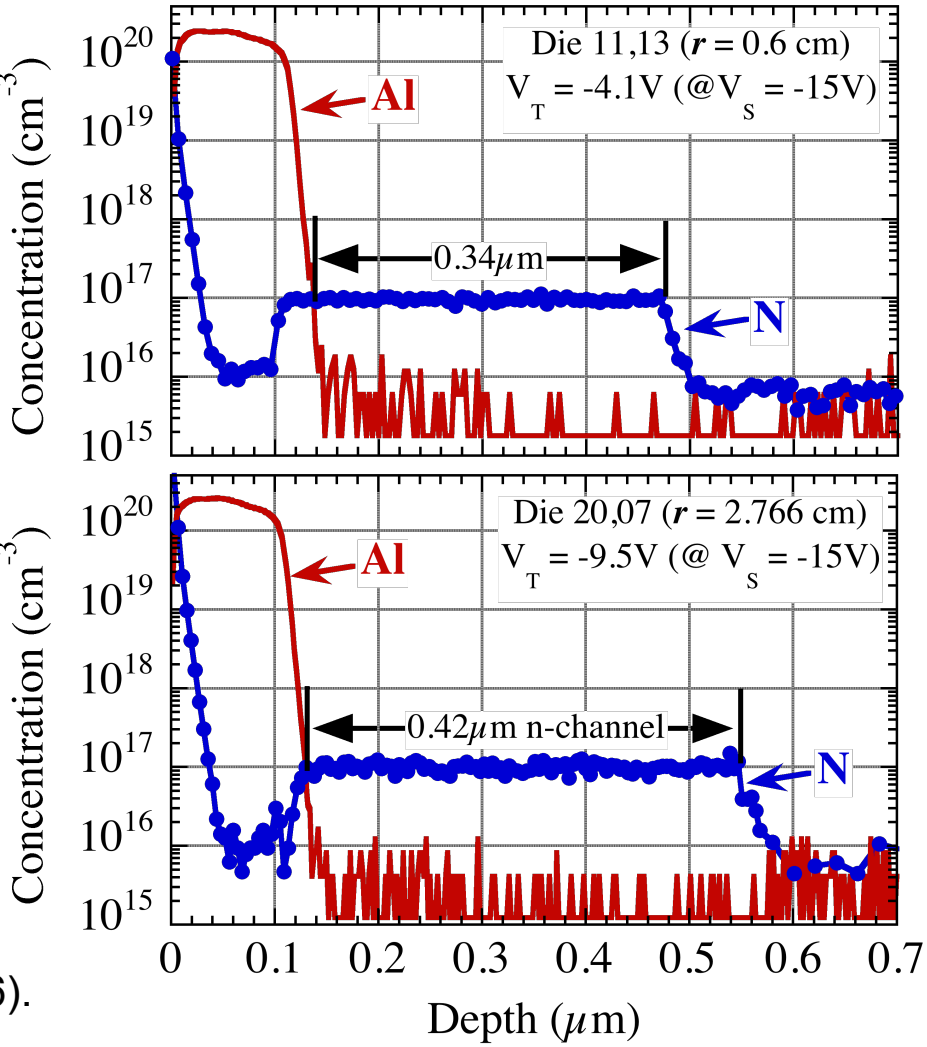
Experimental JFET Threshold (V_T) Non-Uniformity [1]

Wafer 8.1 Measured JFET V_T vs. Radial Distance (***r***) from Wafer Center



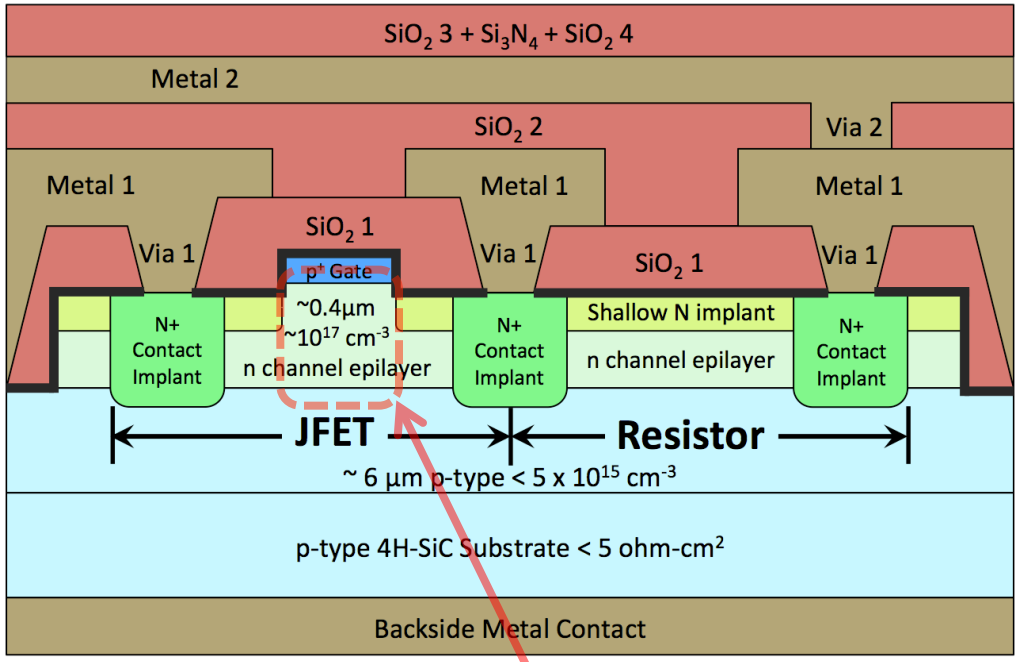
Radial variation of JFET V_T is due to non-uniform <u>thickness</u> in as–grown epilayers.

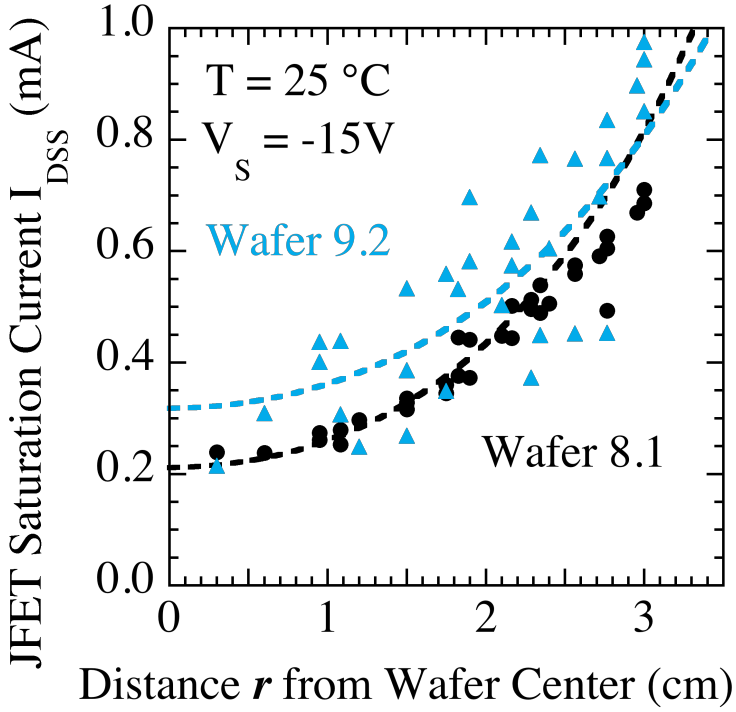
Secondary Ion Mass Spectroscopy Measurement of JFET Epilayer Doping and Thicknesses



[1] Materials Science Forum **858** p. 903 (2016).

Impact of V_T Non-Uniformity on JFET Parameters

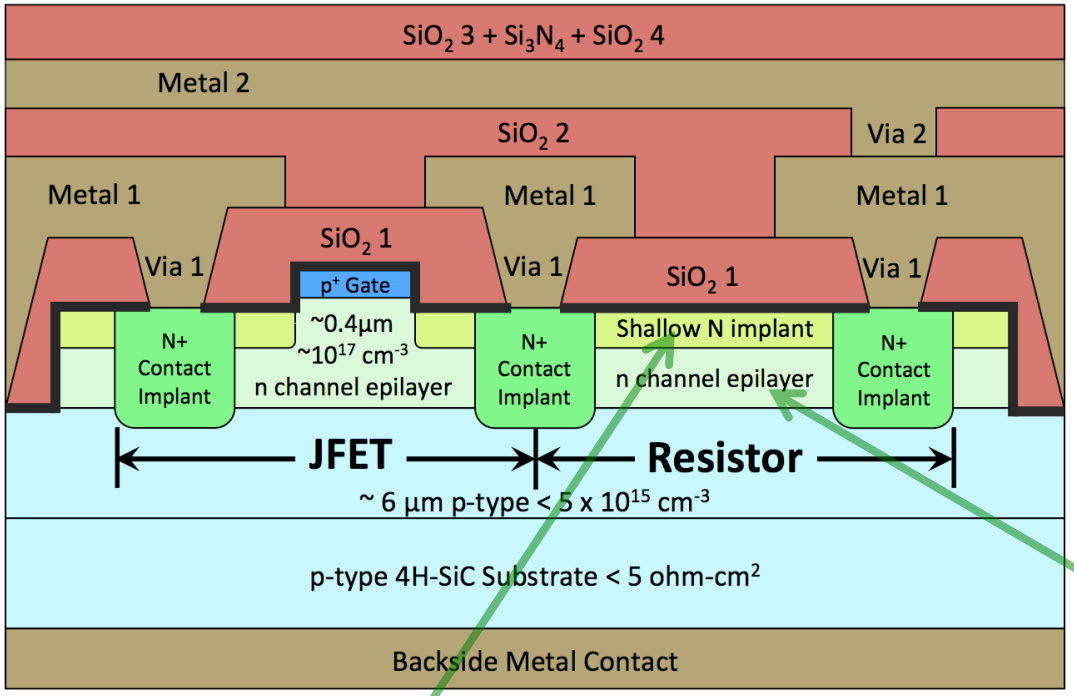




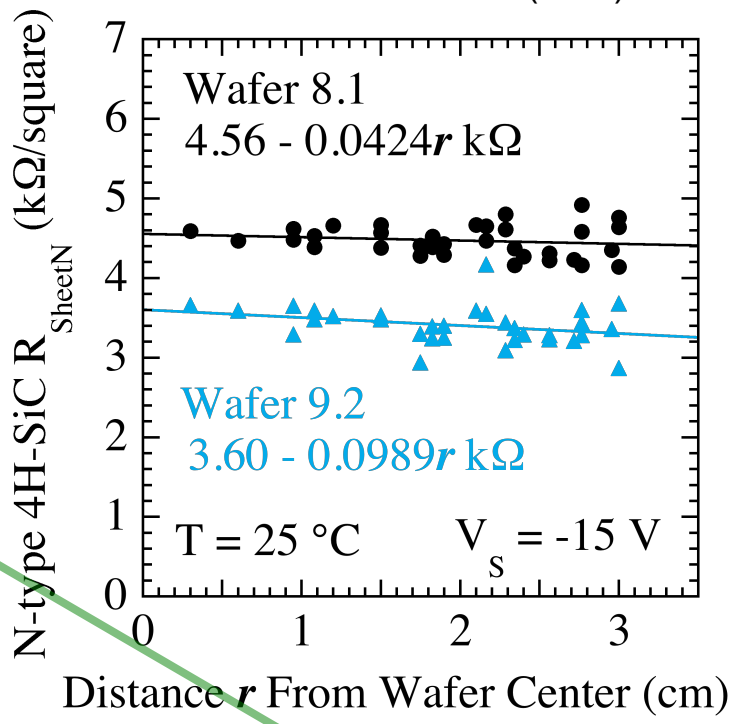
Significant wafer positional dependence in parameters governed by intrinsic JFET n-channel thickness with wafer position.

- Measurements: JFET Saturation current (I_{DSS}), Transconductance (g_{m0}), on-resistance (R_{DS}).
- Models: SPICE NMOS Level 1 Parameters **VTO** and **KP.**

Resistor Dependence on Wafer Position



n-SiC Sheet Resistance (R_{SheetN}) from Transmission Line Method (TLM) data



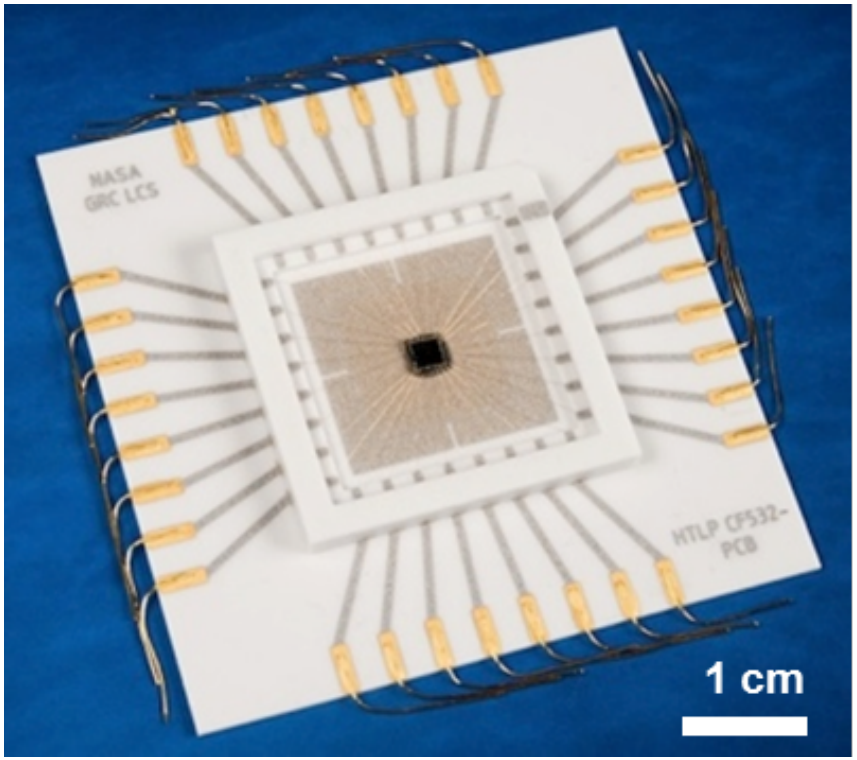
n-SiC resistors exhibit negligible wafer position dependence.

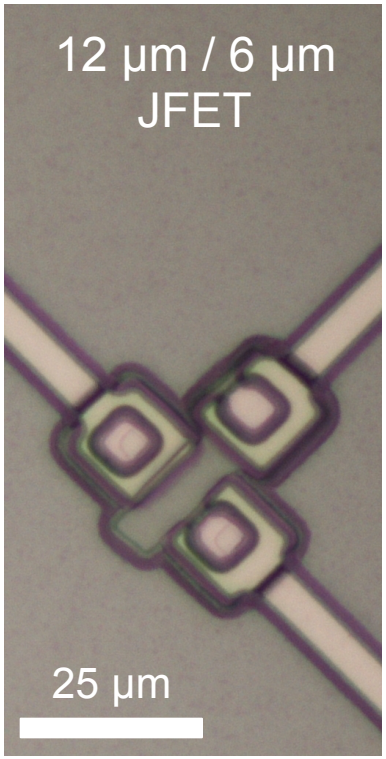
- The shallow N implant is uniform and provides more conductance than n-channel epilayer.
  - Shallow N Implant dose ~ 6 x 10^{12} cm^{-2}.
  - Epilayer N_{Sheet} is ~ 3 x 10^{12} to 4 x 10^{12} cm^{-2} (Wafer 8.1 SIMS).
    - Change across the wafer is ~ 1 x 10^{12} cm^{-2}.

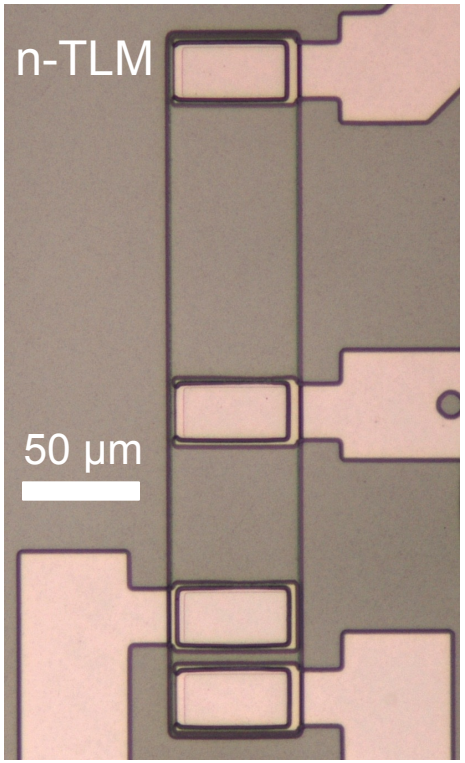
Device Measurements vs. Temperature

High-temperature data measured on chips packaged for prolonged T ≥ 500 °C oven-testing.

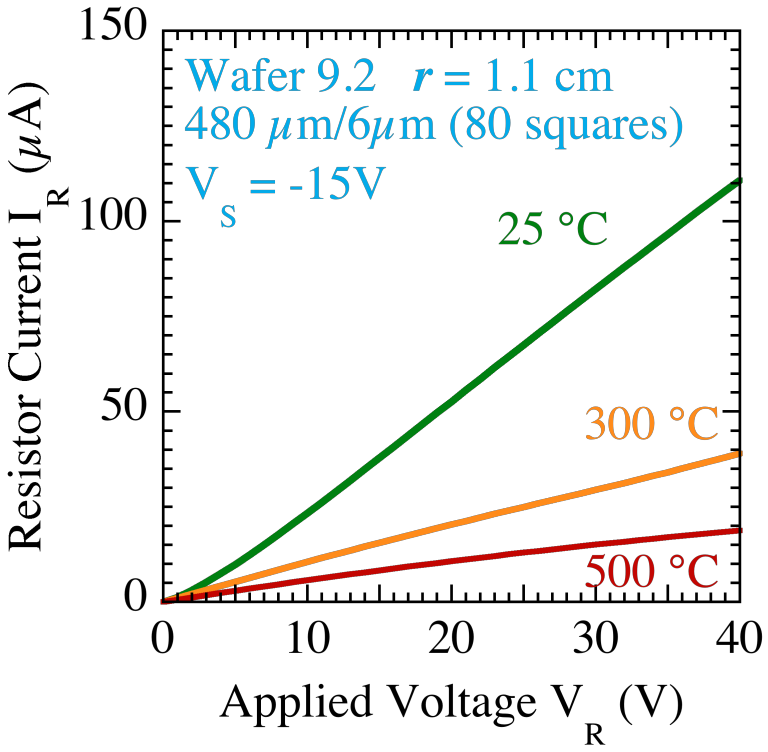
- 32-pin ceramic custom package (L. Chen, HiTEC 2016 Monday TP2 presentation)
- 3 Wafer 8.1 chips with discrete JFET & n-resistor TLM.
- 1 Wafer 9.2 chip with discrete JFET & n-resistor TLM.
- Except where noted, data is from initial T-ramp up to 500 °C (i.e., no “burn-in”)

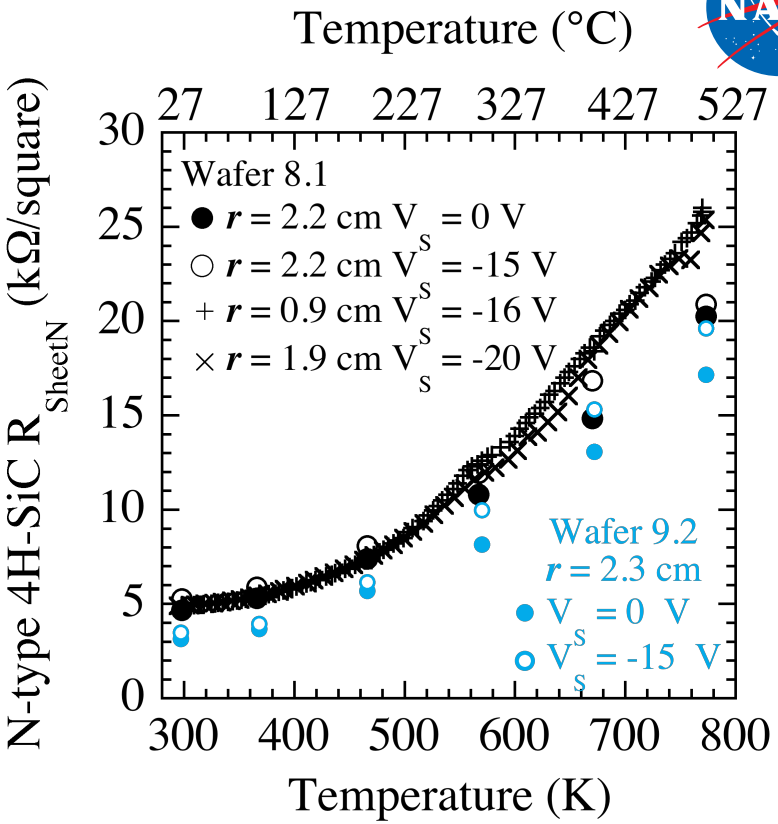






Resistor Dependence on Temperature

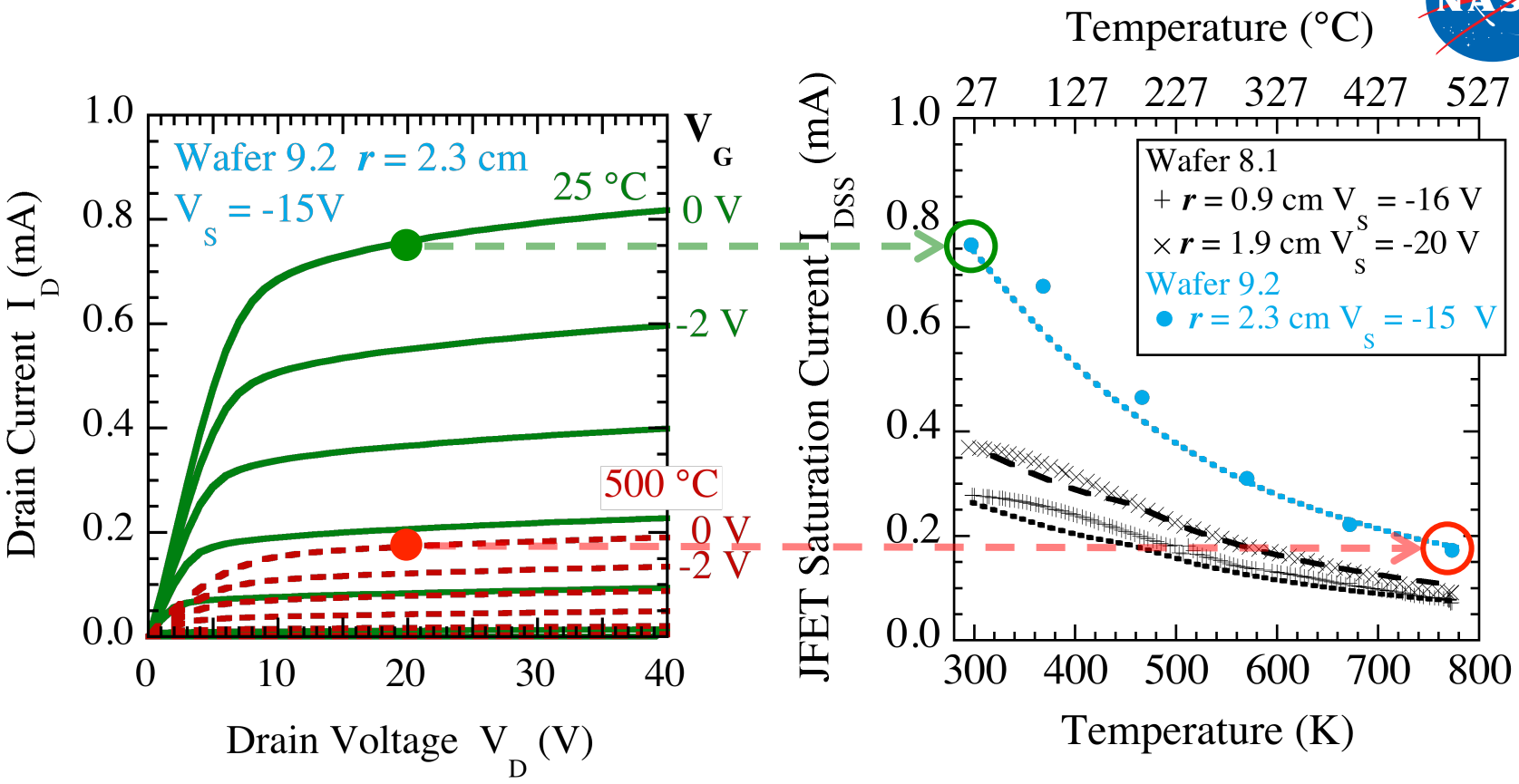




R_{Sheet} (and R) values increases about 5-fold as T increases from 25 °C to 500 °C.

- Consistent to first-order with prior n-type 4H-SiC conductivity vs. T studies.

JFET Dependence on Temperature

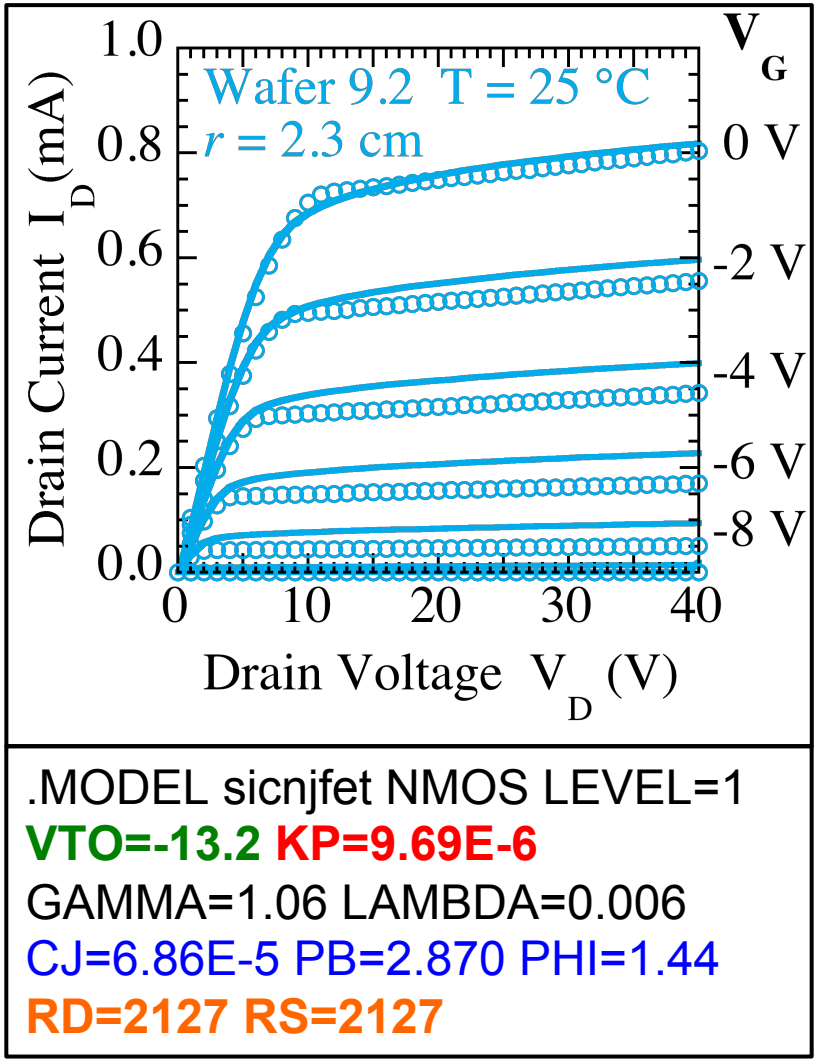


Significant change in JFET parameters with increasing T, consistent with prior works.

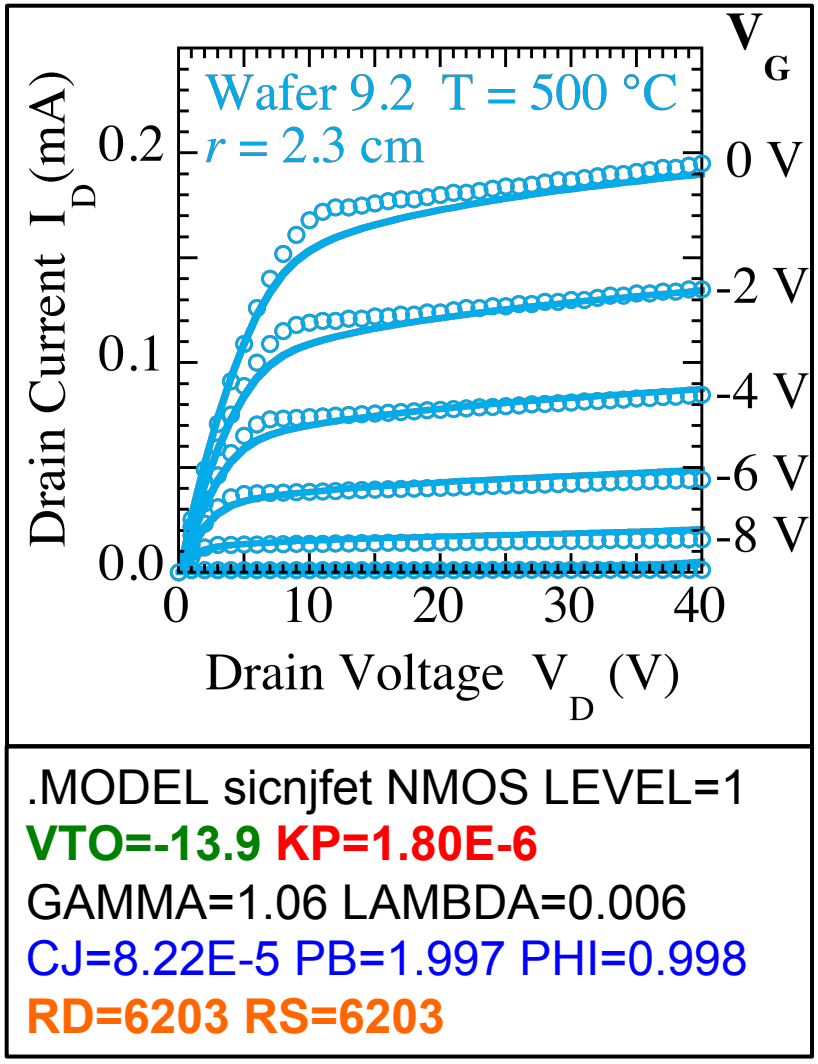
- Some channel mobility loss offset by more negative JFET threshold voltage.

JFET SPICE Model Dependence on Temperature

Lines = Measured Device, Symbols = SPICE

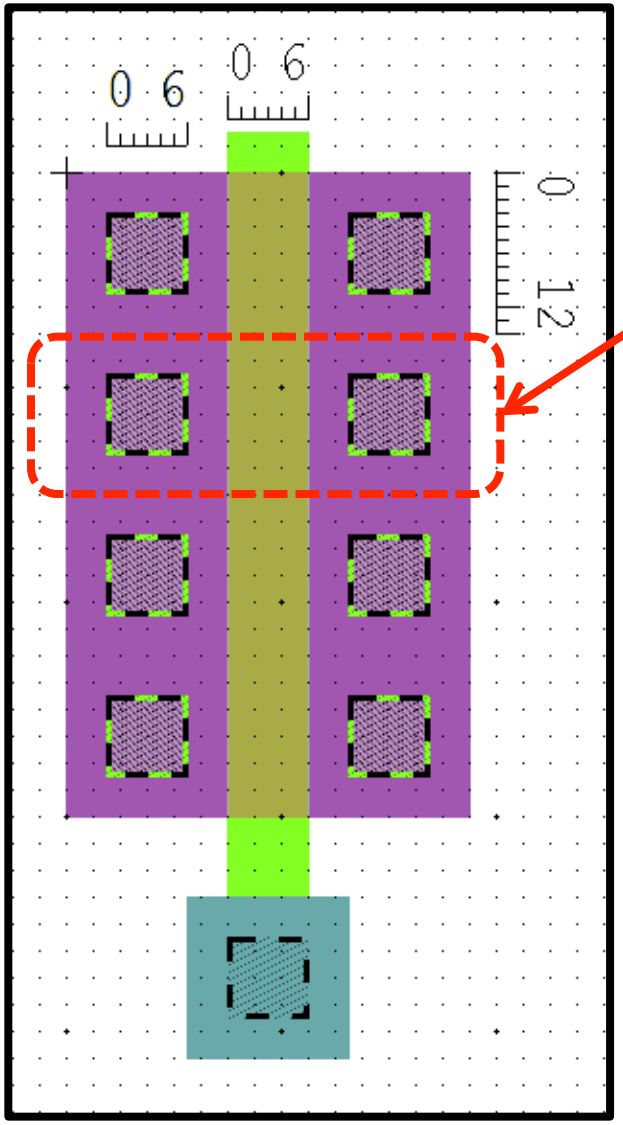


.MODEL sicnjfet NMOS LEVEL=1
VTO=-13.2 KP=9.69E-6
GAMMA=1.06 LAMBDA=0.006
CJ=6.86E-5 PB=2.870 PHI=1.44
RD=2127 RS=2127



.MODEL sicnjfet NMOS LEVEL=1
VTO=-13.9 KP=1.80E-6
GAMMA=1.06 LAMBDA=0.006
CJ=8.22E-5 PB=1.997 PHI=0.998
RD=6203 RS=6203

JFET SPICE Modeling



All JFETs in NASA 4H-SiC IC process have gate length L_G = 6 µm

Gate width W_G = M * 12 µm (M = Integer)

SPICE model accurately represents a “Unit Cell JFET” of dimensions W_G = 12 µm / L_G = 6 µm

Larger JFETs (such as W_G = 48 µm / L_G = 6 µm depicted) are implemented using SPICE parallel instance parameter M (such as M = 4 for this JFET).

Example SPICE text instance of depicted device:

```
MJFET48BY6 D G S B sicnjfet L=6.0E-6
W=1.2E-5 AS=1.8E-10 AD=1.8E-10 M=4
```

TO MAKE LARGER JFETs, CHANGE M ONLY!

- Keep other numbers the same as shown above.

Simplified Circuit Design Modeling

“Layout ratio” based circuits can be designed using a few SPICE model test cases:

- Initial design based on T = 25 °C and ***r*** = 1.5 cm wafer position SPICE models, then verify functionality at T and ***r*** extremes:
- 25 °C at ***r*** = 0 cm (wafer center)
- 25 °C at ***r*** = 3.0 cm (wafer edge)
- 500 °C at wafer center
- 500 °C near wafer edge

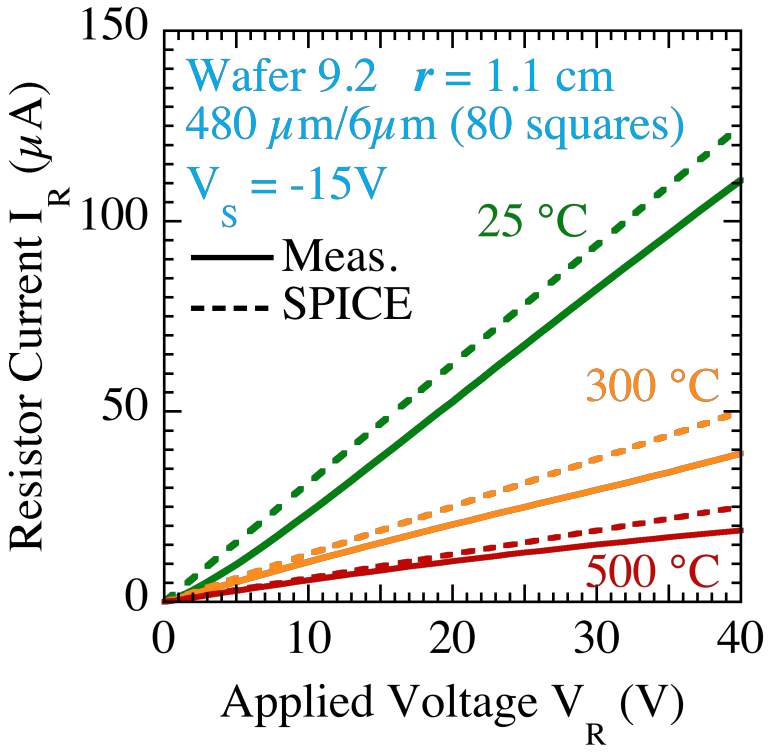
SPICE JFET (NMOS) models for above cases, along with additional cases are listed in the HiTEC 2016 proceedings paper.

- Based on more recent Wafer 9.2.

Modest adjustments to power supply voltages needed with device position on wafer.

- Due to wafer position dependence of V_T.
- Supply voltages change from ~ 25 V at center to ~ 30 V near edge (Wafer 9.2).
- No supply voltage adjustment with T for devices with linear & uniform ohmic contacts.
- Some output voltages and AC performance characteristics also change with device position (circuit-specific).

Simplified 4H-SiC n-Resistor SPICE Modeling



T (°C)	Resistor SPICE Model Text
25	.MODEL sicnres R RSH=4000
300	.MODEL sicnres R RSH=10000
500	.MODEL sicnres R RSH=20000

Example SPICE text lines that implement 80-square resistor at T = 500 °C

```
RTEST n1 n2 SICSEMIR L=4.8e-04 W=6.0e-06
.MODEL SICSEMIR R RSH=20000
```

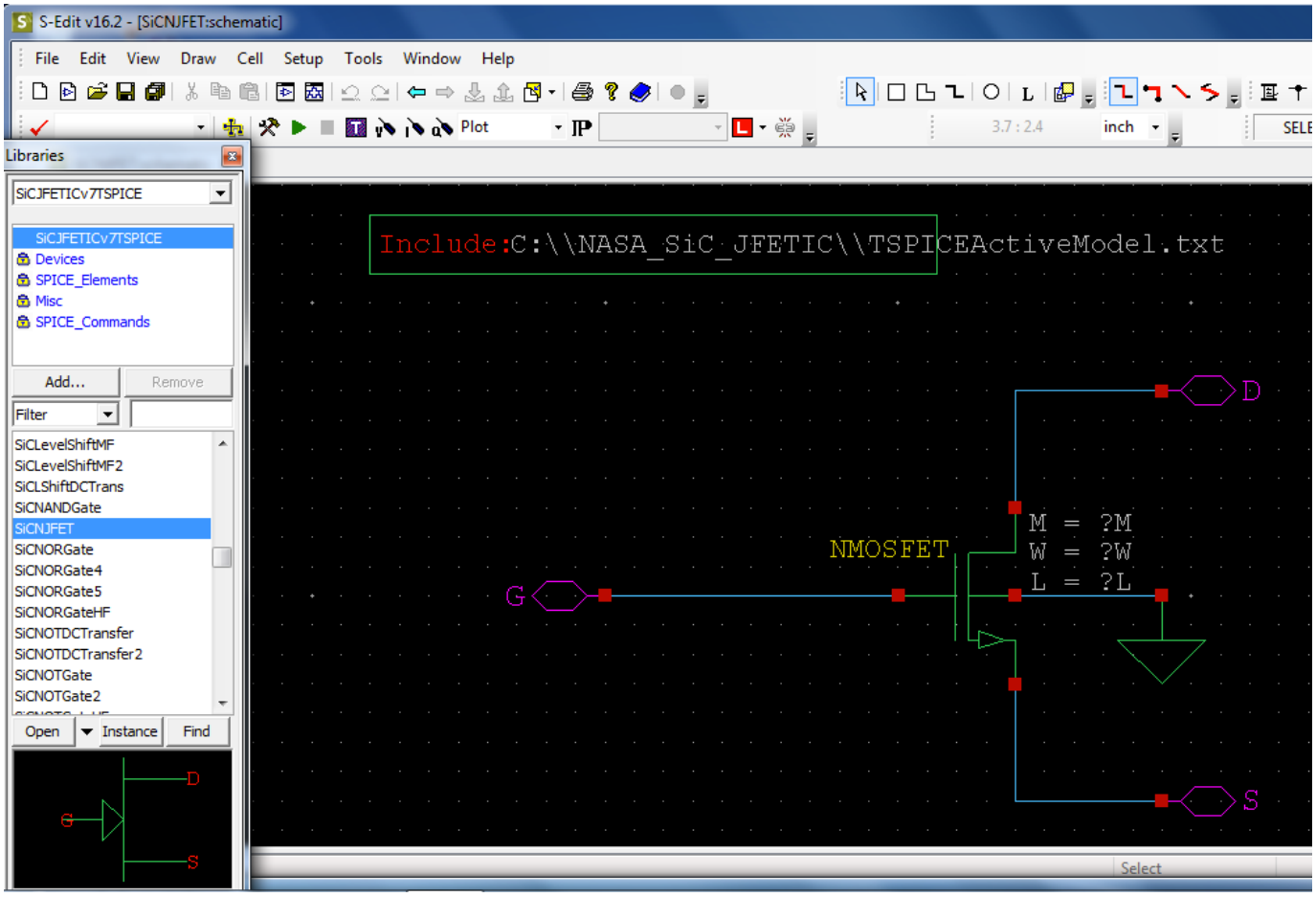
The baseline SPICE semiconductor sheet resistance model is accurate to first order.

- Only temperature dependence is needed, since sheet resistance is uniform over wafer.
- Resistor geometries (much longer than 6 μm width) minimize contact resistance effects.
- Substrate body bias effect is neglected for baseline SPICE resistor model.
  - Shallow n-implant reduces change in resistance from body bias effect.
  - Improved-accuracy modeling should include body bias effect (future work).

SPICE User Inteface

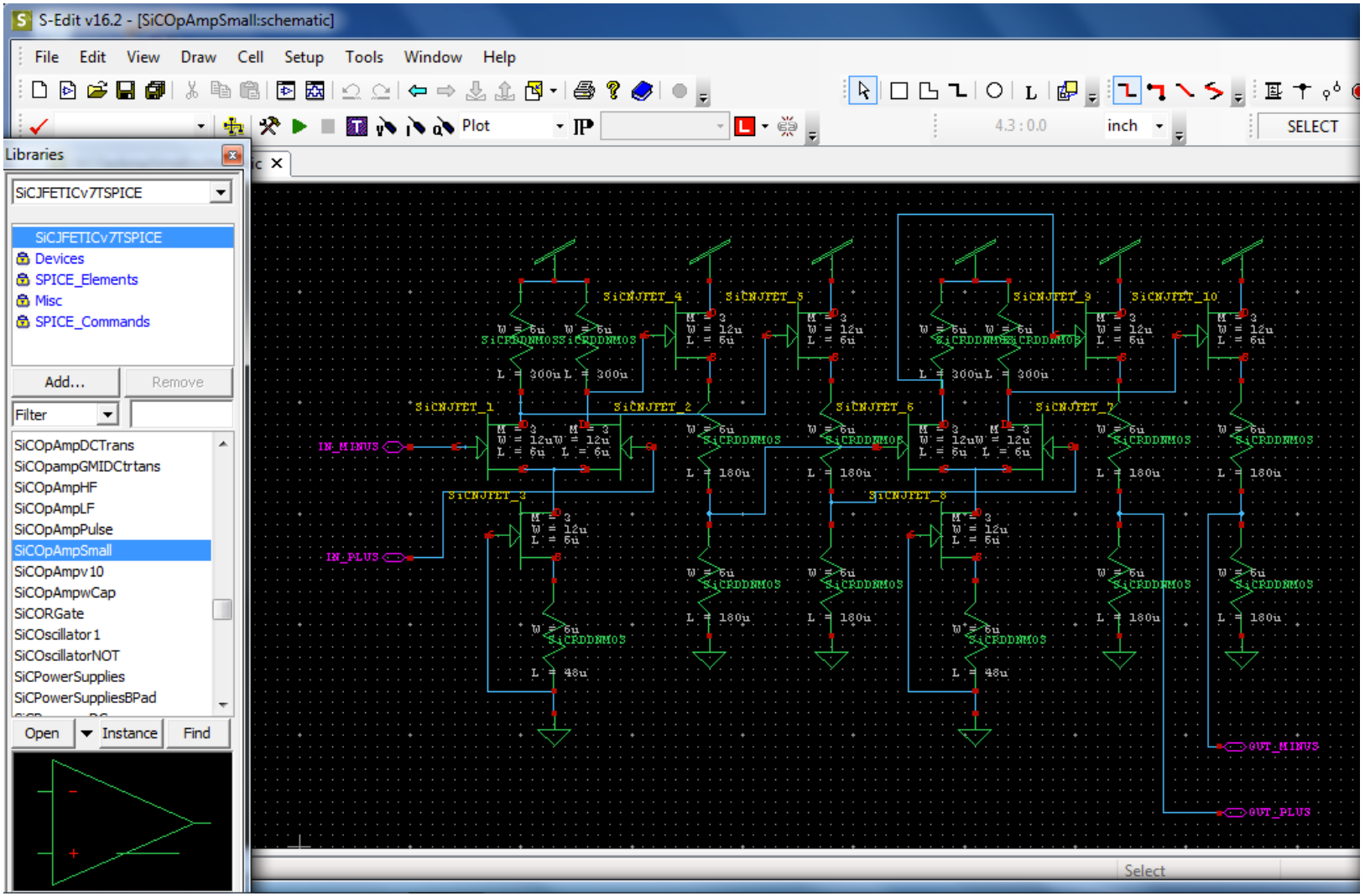
SPICE ".INCLUDE" file can facilitate rapid swapping of various JFET and resistor models (i.e., wafer position and temperature cases).

- Simple program can have user choose desired ***r*** and T, then place corresponding models into to the .INCLUDE file read by SPICE.



SPICE User Inteface

Reference base JFET and resistor cells to design more complex integrated circuits.
(Fully differential operational amplifier)



NASA 4H-SiC JFET Integrated Circuit Design Guidelines

N-Channel JFETs and n-channel resistors using presented SPICE models.

- Single-chip device counts of a few hundred or less.
- Single-JFET on-current of 100 mA or less, blocking 50 V or less.
- Use multiples of 12 μm / 6 μm unit-cell JFET, 6 μm wide resistors.

Layout ratio based circuits to accommodate systematic electrical parameter variations

Signal input and output voltages between 0 to -10 V.

Signal currents larger than 10 μA (well above measured 500 °C leakages).

Power supplies: VDD from +25 V to +30 V, GND, and VSS from -25 V to -30 V.

- Chip backside must be tied to –VSS (package must accommodate this).

Conservative (kHz) operating frequencies (except for ring oscillators).

32 input/output pins (including power) on a chip.

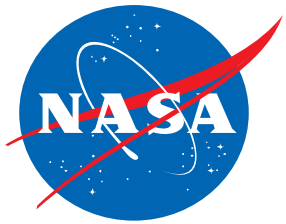
Prototype integrated circuit designs meeting above guidelines could be fabricated by NASA Glenn Research Center (under negotiated collaborative Space Act Agreement).

Summary

NASA Glenn 500 °C durable JFET IC devices can be modeled to first-order accuracy using commonly available versions of SPICE.

Models in this presentation were used with commercial and non-commerical SPICE programs to design prototpye 500 °C durable ICs demonstrated at NASA Glenn.

Prototype IC designs meeting 4H-SiC JFET IC guidelines could potentially be fabricated by NASA Glenn (under negotiated collaborative Space Act Agreement: https://technology.grc.nasa.gov, Priscilla.S.Diem@nasa.gov).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